

# Datasheet

## **GW8811**

Based on the ARM® Cortex®-M0

Bluetooth 4.2 Ultra-low Power SoC

Version: V1.0.1

# 1 Product Features

## 1.1 General Description

The GW8811 is an ultra-low power Bluetooth 4.2 SoC based on the 32-bit ARM® Cortex®-M0 core, integrated with high-performance 2.4GHz RF transceiver and rich digital interfaces. With on-chip Balun, there is no need for off-chip impedance matching network and external crystal oscillator load capacitance, which minimize BOM cost and PCB area. A high-efficiency DC-DC step-down converter is integrated to realize ultra-low power consumption.

## 1.2 Key Features

- Fully qualified Bluetooth Low Energy 4.2 standard
- Based on ARM®Cortex®-M0 core
- Frequency: 64MHz
- 2.4GHz RF transceiver
- 8 channel 1MSPS 10-bit SAR ADC
- Support OTA
- 32MHz and 32.768kHz crystal oscillator
- Built-in buck DC-DC converter
- 64MHz and 32.768kHz RC oscillator
- Quadrature Decoder
- Support ISO7816 interface
- Infrared emitting and receiving
- Communication interface options

- Master I<sup>2</sup>C x2
- Master Three SPI & Four-Wire SPI
- UART x2
- Digital peripherals
  - PWM x6
  - RTC
- configurable GPIO features
- Serial Wire Debug(SWD) supported

## 1.3 Applications

- Intelligent wearable
- Smart home
- Remote controller
- Health applications
- HID devices

## 1.4 Key Parameters

Parameter	GW8811KEU6	GW8811CEU6
Max. TX Power	+4 dBm	+4 dBm
RX Sensitivity	-94dBm	-94dBm
TX Current	4.8 mA@0dBm	4.8 mA@0dBm
RX Current	2.8 mA@0dBm	2.8 mA@0dBm
Sleep Mode Current	2.7µA	2.7µA
Deep Sleep Mode Current	1 µA	1 µA
Flash	512 kB	512 kB
Data RAM	24 KB	32 KB
Supply Voltage	1.8~3.6 V	1.8~3.6 V
GPIO	21	32
Operating Temperature, Tj	-40~+85 °C	-40~+85 °C
Package(mm)	5.0 x 5.0 x 1.0	5.0 x 5.0 x 1.0

\*Condition: V<sub>DD</sub>=3V, DCDC enable.

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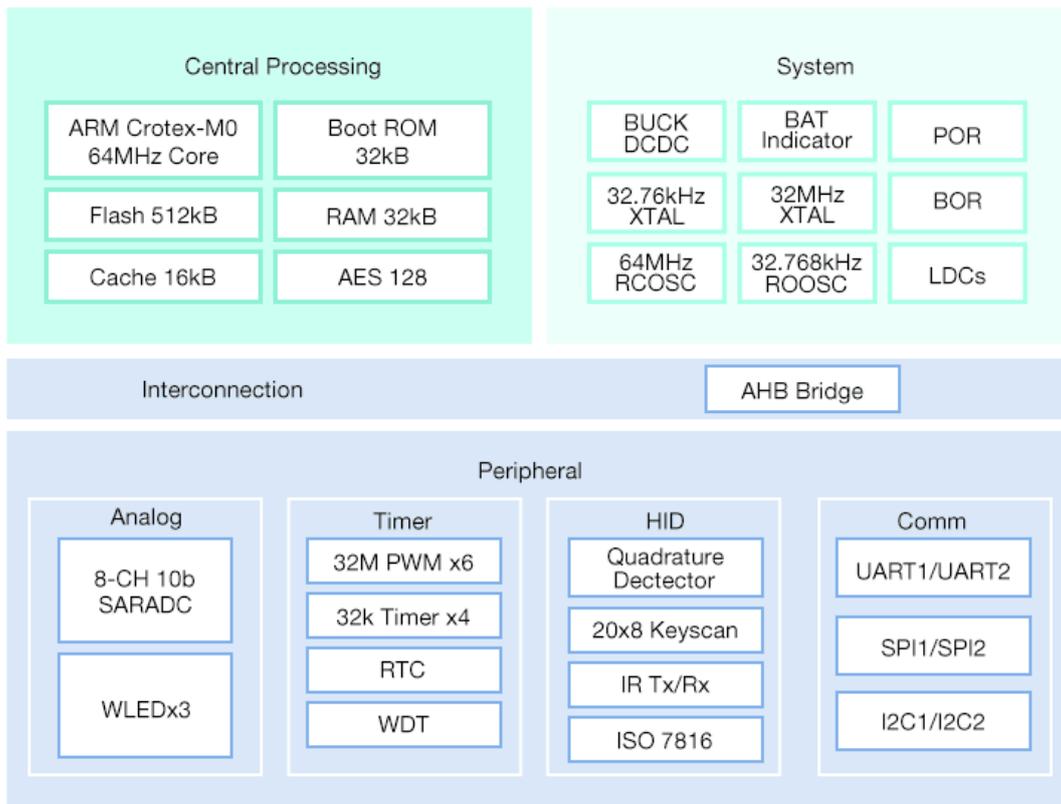
## 2 Introduction

### 2.1 Overview

The GW8811 chip is highly integrated with 32-bit ARM® Cortex®-M0 processor, Radio Transceiver, Bluetooth Modem, Bluetooth 4.2 baseband, Flash and SRAM, on-chip Balun and digital interfaces such as SPI/I<sup>2</sup>C/UART etc. The ARM® Cortex®-M0 processor can operate at the highest clock rate of 64MHz for heavy thread computing applications, and can also operate at lower clock rate for simple data communication purpose. A built-in DCDC converter is integrated to provide full-solution SoC for stand-alone applications such as IoT and wearable devices.

Shows the architecture block diagram of the chip. Refer to the subsequent chapters for detailed information on the functionality of the different interface blocks.

Figure 1.Functional Block Diagram



## 2.2 Terminology

Table 1. Terminology

Term	Description
GND	Ground
BiDir	Bi-Directional
PWM	Pulse Width Modulation
HID	Human Interface Device
GPIO	General Purpose Input / Output

## 3 Function description

### 3.1 ARM® Cortex®-M0

ARM® Cortex®-M0 processor is the smallest ARM processor available. It provides ultra-low power consumption and minimal code of the processor to enable developers to achieve 32-bit performance. With its friendly architecture, users can develop applications easily and fast.

GW8811 series supports dynamic clock technology for various applications ranging from 8MHz to 32MHz. The CPU clock can be configured to use internal 64MHz RC clock or 32MHz crystal clock. When using RC clock, MCU can run independently with Bluetooth link-layer and switch on and off at users' discretion. When using 32MHz crystal clock, it should follow the working period of Bluetooth (the Bluetooth working period can be determined by MCU).

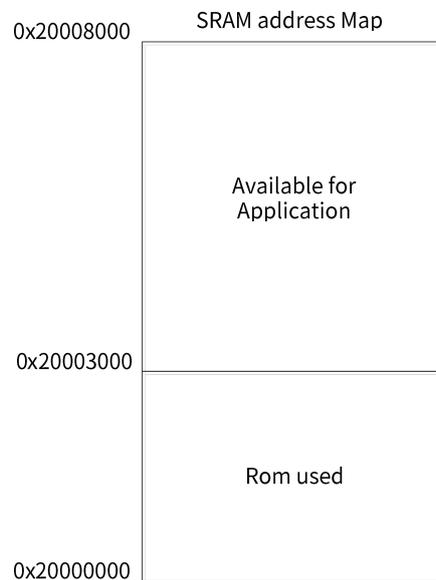
SWD (Serial-Wire Debug) is supported for powerful debug and trace features with two connection pins.

GW8811 has 24KB ROM for boot-up and BLE protocol stack, 512KB flash for profile/application, and 32kB exchange/data SRAM.

## 3.2 Memory

- ROM: 32kB internal ROM is for the Boot code and Bluetooth Low Energy protocol stack firmware.
- Data RAM: 32KB Data RAM is integrated, 12KB will be used up by ROM(BLE stack), 20kB is available for application.
  - 0x2000 0000 ~ 0x2000 3000 (12kB) is used by ROM.
  - 0x2000 3000 ~ 0x2000 8000 (20kB) is available for application
- Flash: 512kB flash is integrated for code and firmware storage.

Figure 2.Data SRAM Address Map



## 3.3 Bluetooth Low Energy Core

The Bluetooth Low Energy Core of GW8811 is SIG Qualified. It is fully compliant with Bluetooth Smart v4.2 slave-role controller and provides qualified features as below:

- Bluetooth low energy stack: All layers up to GATT including (PHY, LL, HCI, L2CAP, GAP, SM, ATT/GATT)
- Slave-Role Link layer
  - Slave-required PDU types
  - Encryption/Decryption
- L2CAP

- Slave connection update
- Attribute channel
- Security channel
- GAP/ATT/GATT: Mandatory protocols
- Security Management
  - Key generation and passing
  - Automatic security engine
- DTM: For RF qualification
- Profile configuration
  - Initialization
  - Flexibility and testability

### 3.4 Radio Transceiver

The GW8811 series integrates high performance 2.4GHz radio transceiver for Bluetooth radio specification. With the built-in on-chip balun, GW8811 does not need external balun circuit to minimize BOM. The integrated high efficiency PA can transmit up to +4dBm RF power for class 2 operation, while the integrated low-IF receiver can provide excellent sensitivity up to -94dBm and outstanding ACI interference rejection capability for good receptivity in the complex working environment of 2.4ghz ISM band.

### 3.5 Power Management

The GW8811 series integrates a power management unit for handheld or wearable devices with DCDC converter. The DCDC converter transforms battery voltage to a lower/higher internal voltage with minimal power loss. The DCDC converter could provide excellent power efficiency with adaptive loading current setting. The DCDC Buck converter can be bypassed when the supply voltage drops to the lower limit of the voltage range, and external DCDC converter is also supported. It can provide power solution for one-cell Lithium-Ion, one-cell or two serial alkaline battery applications where the output voltage is adjustable, 1.15V~3.6V.

### 3.5.1 DCDC Buck Converter

Higher performance DCDC Buck converter would bring up better battery life time. To ensure longest battery life, Buck converter has an optional bypass mode under light load current. The reduction in supply voltage level from a high voltage to a low voltage reduces the peak power drain from the battery. For better conversion efficiency, DC resistance (RDC) should be less than 0.25ohm.

Figure 3. DCDC Buck Converter Configuration

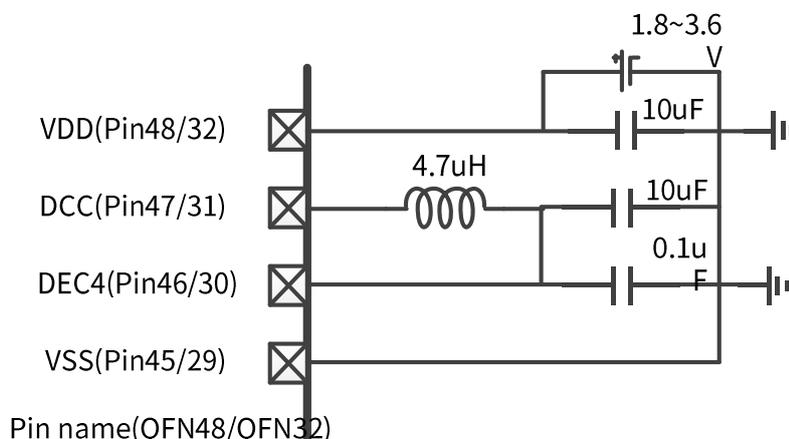


Table 2. Buck Converter Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Voltage	$V_{In,Buck}$	1.8	3.3		V	
Output Voltage	$V_{DCDC,Buck}$	1.8	3.3		V	
Converting Efficiency	$Eff_{Buck}$		88		%	@20mA Loading current
Maximum Load Current	$I_{Load,Buck}$			40	mA	
Output Ripple Voltage	$V_{RIPPLE,Buck}$		30		mV	

### 3.6 Power States & Sequence

Table 3. Operation Mode

State	Functional Description
Deep sleep	All power supplies are off except retention cell and I/O for pin wake-up. All clocks are gated.
	System can be woken up by configured external pin. When it

	happens, GW8811 series of chips are reset from boot-up state.
Sleep	Active clocks (32MHz xtal and 64MHz RCOSC) are off, and the sleep clock (32.768kHz) remain working. Certain engines' power are off.
	Two types of sleep modes are provided in GW8811. When CPU uses internal 64MHz RC clock, it can set CPU sleep mode independently and woken up by timer or Bluetooth interrupts. When CPU uses 32MHz crystal clock together with Bluetooth, it follows Bluetooth sleep mode aligning to connection interval.
Standby	This is the default state after power-up. All clocks are working but the RF is inactive.
TX	This mode is entered when Bluetooth link-layer determines to send transmission packets.
RX	This mode is entered when Bluetooth link-layer determines to receive an incoming packet.

### 3.7 GPIO

GW8811 series offers maximum 32 GPIOs and 2 SWD debug ports (SWDCLK, SWDIO). SWDCLK and SWDIO pins should be pulled low during GW8811 booting procedure.

GPIO features:

- Configurable output drive strength
- Optional internal pull-up resistors
- Configurable input polarity
- Support both high or low level triggered pin wake-up
- Each GPIO can be individually mapped to any digital function for layout flexibility
- Hardware de-bounced GPIO

### 3.8 Timer

GW8811 series provides 4 low speed Timers, Timer0~Timer3 are running with 32.768KHz clock from 32.768KHz crystal oscillator clock or 32KHz RC clock. Timer interrupt can wakeup CPU from sleep mode. Timer3 is reserved for Rom Code. GW8811 also provides a high speed timer.

### 3.8.1 Low Speed Timer

GW8811 series provides 4 low speed timers with 32-bit width.

Timer0~Timer3 are running with 32.768kHz clock from XTAL or LPO.

Timer interrupt can wakeup CPU from sleep mode. Timer3 is reserved for Rom Code, not for external application.

### 3.8.2 High Speed Timer

The high speed timer works with the 32MHz RC clock, which has 16-bit width for high speed and accurate timing application. Two operating modes are provided, one-time or continuous, an interrupt to MCU can be triggered by timer at the end of period.

## 3.9 Real Time Clock (RTC)

GW8811 series offers an RTC timer for real time clock application.

### 3.10 Watch Dog Timer (WDT)

GW8811 series offers one 16-bit countdown watchdog timer for supervisor purpose. It also runs at 32.768kHz clock for maximum 2sec supervisor time to execute system reset due to a hardware fault or program error.

### 3.11 SW Encryption

GW8811 series offers 48bits encryption key for flash code protection.

### 3.12 AES Encryption Engine

The AES engine accelerates the algorithm calculations that are needed for implementing the user defined security algorithm. The AES encryption block supports 128 bit AES encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption.

## 3.13 Peripheral

### 3.13.1 UART

The GW8811 series has two sets of UART interface (UART0, UART1) for serial

asynchronous communication between devices. UART-0 has CTS/RTS hard flow control for option. Data frame configuration is as eight (8) data bits, with parity bit, and one (1) stop bit shown figure below.

Figure 4. UART Data Frame

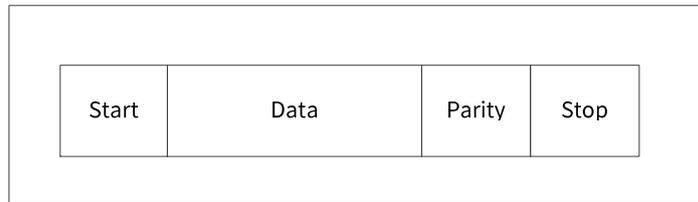


Table 4. UART Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Baud Rate	BR	1200		921600	bps	
Baud Rate Accuracy	BR <sub>ACCU</sub>			3	%	

### 3.13.2 I<sup>2</sup>C

The GW8811 series has two sets of I<sup>2</sup>C interface (I<sup>2</sup>C\_0, I<sup>2</sup>C\_1) for 2-wire bi-directional communication between devices. The I<sup>2</sup>C supports wide range of data rate from 31.25kHz to 1000kHz in register controls. Multiple Read modes are supported as current read, random read, and sequential read. Write mode also support byte write and page write.

Figure 5. I<sup>2</sup>C Control Byte Format

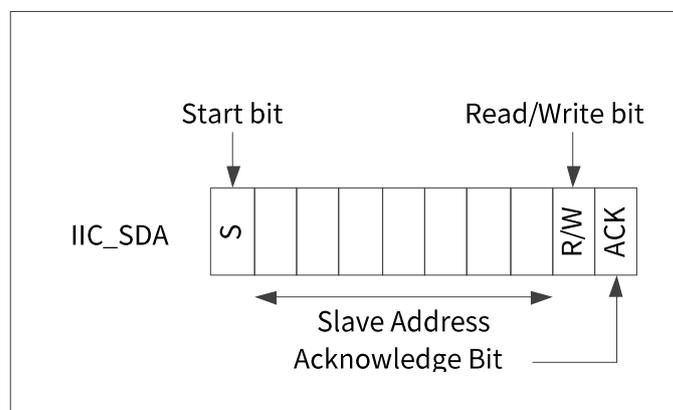


Figure 6. I<sup>2</sup>C Byte Write Format

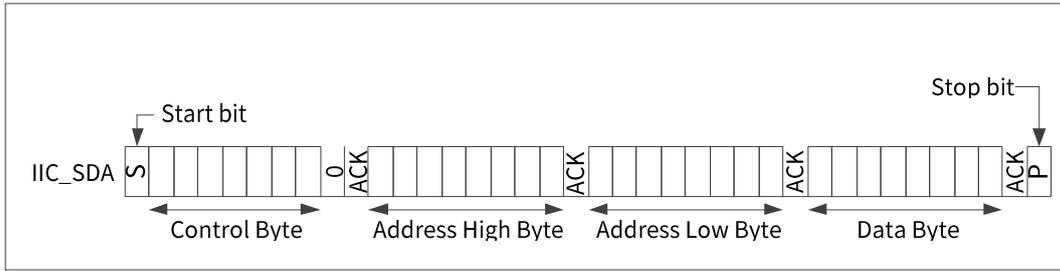


Figure 7. I<sup>2</sup>C Page Write Format

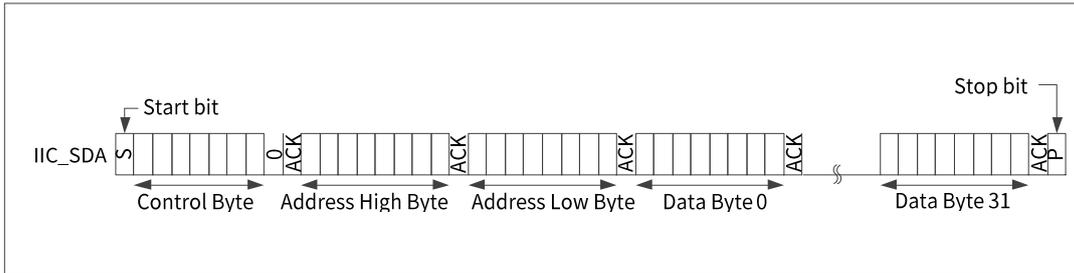


Figure 8. I<sup>2</sup>C Current Read Format

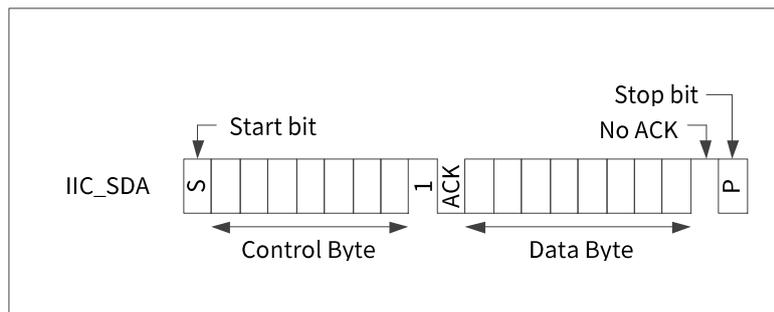


Figure 9. I<sup>2</sup>C Random Read Format

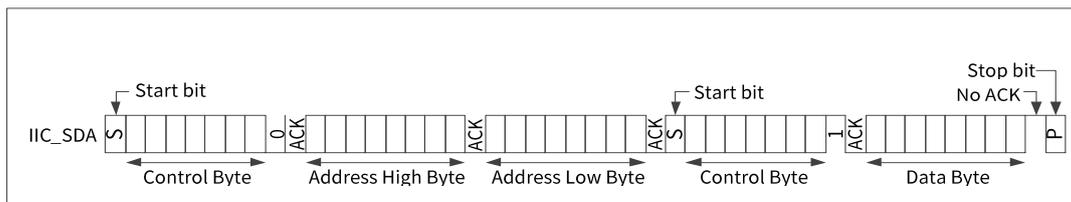
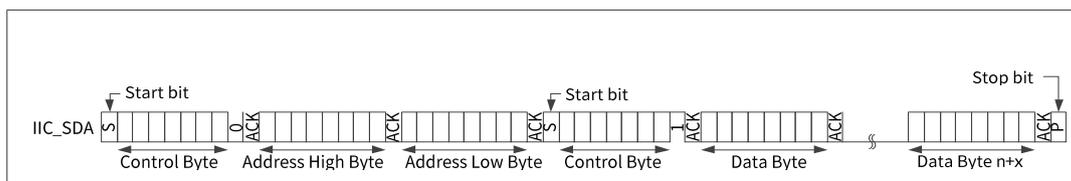


Figure 10. I<sup>2</sup>C Sequential Read Format



### 3.13.3 SPI

The GW8811 series provides two configurations of SPI interfaces. One is four wire SPI, as CSN (chip select), SCLK (clock), SDI (MOSI data) and SDO (MISO data) and the other is two or three wire SPI interface as CSN (chip select) – optional, SCLK (clock), SDIO (bi-directional Data). These two configurations are for master operation only, slave mode is not supported.

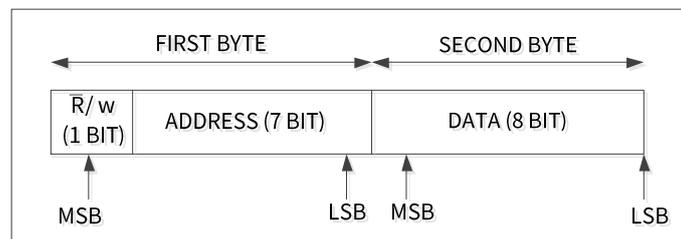
#### Packet Formats

The transmission protocol consists of the two operation modes:

- Write Operation.
- Read Operation.

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has bit-7 as its MSB to indicate data direction. The second byte contains the data.

Figure 11. Four-wire or Three/Two-wire SPI Transmission Protocol



#### Write Operation

A write operation is always initiated by the GW8811 series and consists of two bytes, which the data is going from the host controller to the device. The first byte contains the 7 bits address and has a “1” as its MSB to indicate data direction. The second byte contains the full 8 bits data. The communication is synchronized by SCLK. The GW8811 series changes SDIO or SDI on the falling edges of SCLK and the device reads SDIO or SDI on the rising edges of SCLK.

Figure 12. Four-wire SPI Write Operation

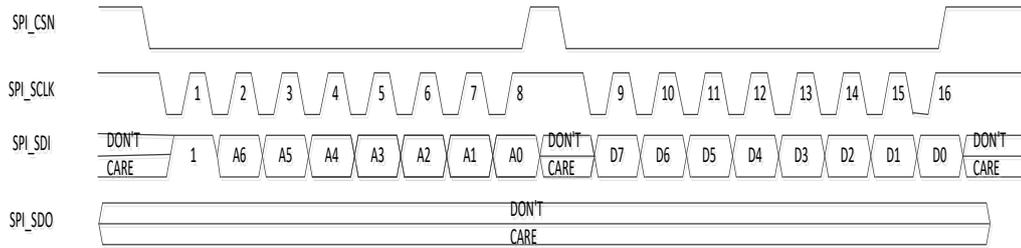
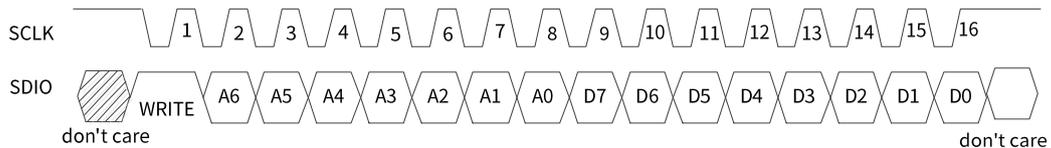


Figure 13. Three/Two-wire SPI Write Operation



### Read Operation

A read operation is initiated by the host controller and consists of two bytes. The first byte contains 7-bit address specified by GW8811 and has a “0” as its MSB to indicate data direction. The second byte contains the full 8 bits data and is driven by the slave device. This communication is synchronized by SPI\_SCLK. For three/two-wire SPI, SDIO is changed on the falling edges of SCLK and is read on every rising edge of SCLK. GW8811 release SDIO bus and handover the control of SDIO bus to the device on the falling edge of last address bit.

Figure 14. Four-wire SPI Read Operation

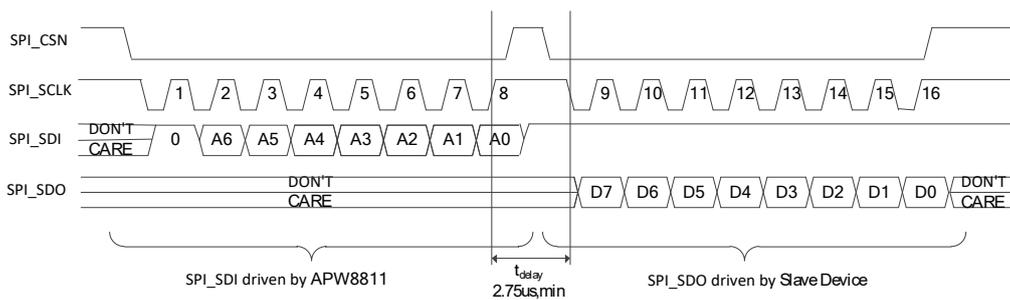
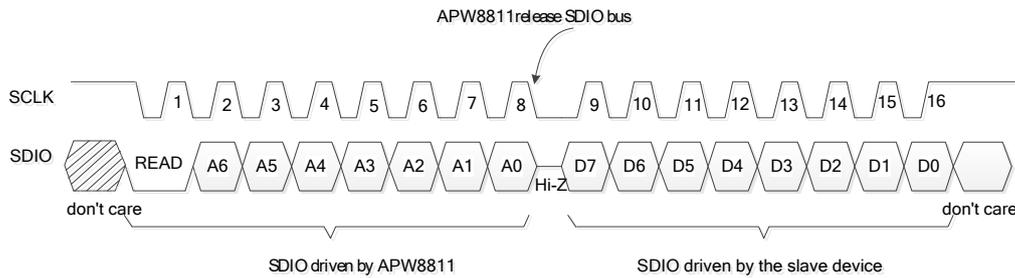


Figure 15. Three/Two-wire SPI Read Operation



### 3.13.4 General Purpose ADC (SAADC)

The GW8811 series integrates a low power 10-bit general purpose Analog-to-Digital Converter (GPADC) with 1MHz sampling rate. It can operate as a 9-channel ADC by switching the GPADC input. One channel is for internal Battery Voltage detection (VDD), while the other eight are configured to monitor eight GPIOs. For better accuracy, internal reference voltage calibration is preferred. Sensing applications as battery monitoring, temperature resistor, analog signal sampling could be applied with this GPADC.

### 3.13.5 ISO-7816-3

GW8811 series integrates one Smart Card Controller supports asynchronous 3V smartcards. The device is controlled by an ISO 7816-3 interface and is capable of card activation, deactivation, cold/warm reset, ATR parsing and data exchange.

- Compliant to ISO/IEC 7816-3: 1997
- Supports FIFO 8 bytes
- Interrupt report
- Flexible clock frequency and baud rate
- Parity/error check and resend
- T=0 protocol
- Wait time configuration
  - ATR wait time
  - Reset time

- Guard time

Figure 16. Function block of ISO7816

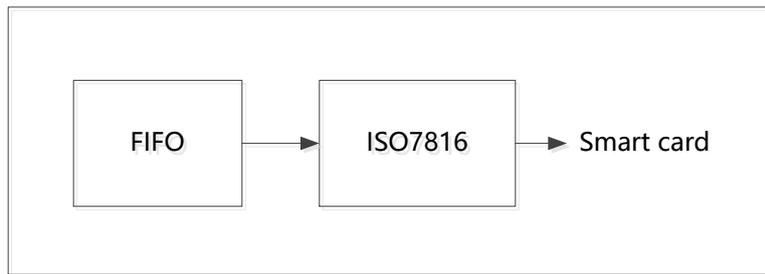


Figure 17. Activation, Cold Reset and ATR

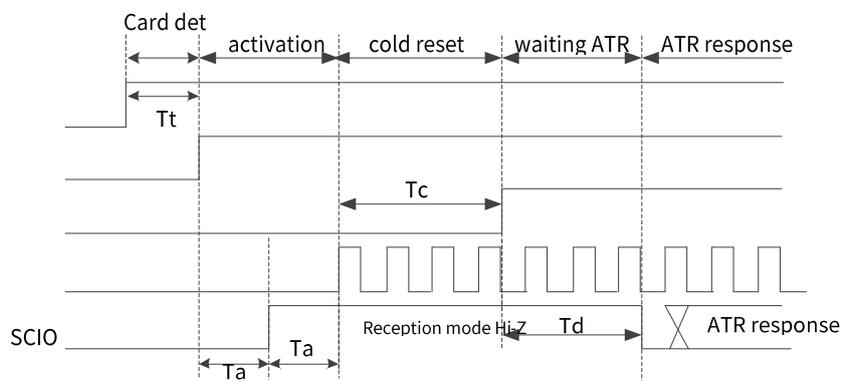
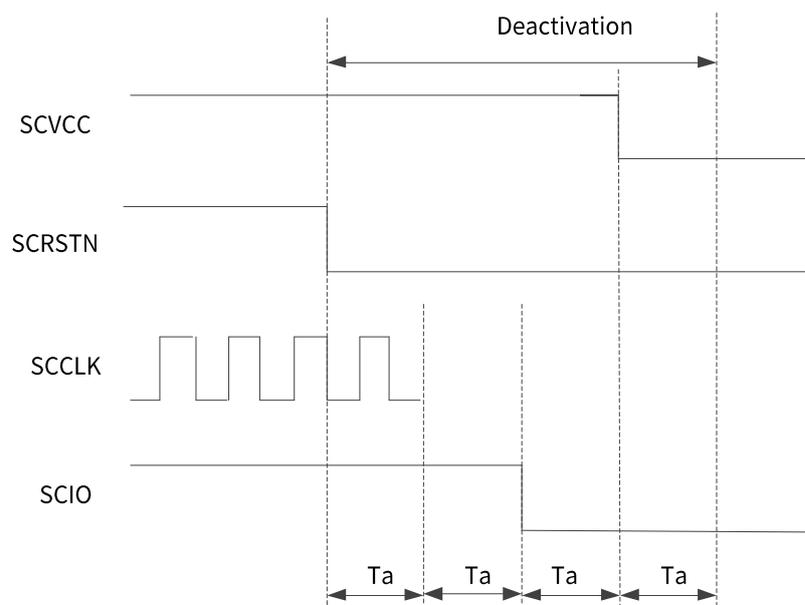


Figure 18. Deactivation Sequence



### 3.13.6 IR Transmitter and Receiver

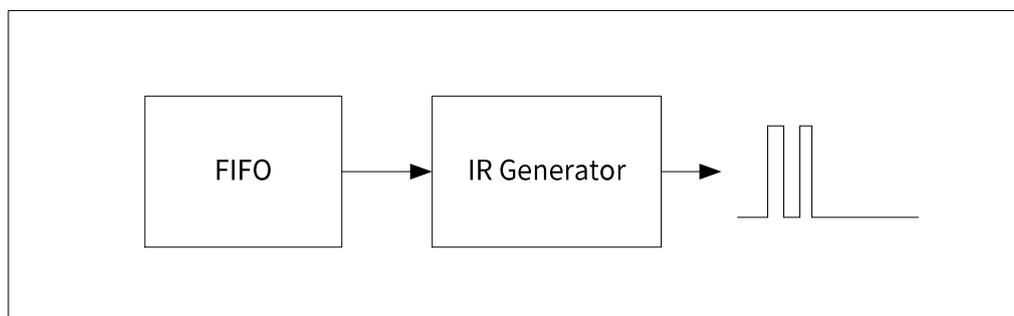
GW8811 series integrates an IR transmitter and Receiver for remote controller applications.

#### IR Transmitter

The Infrared generator provides a flexible way of transmitting any IR code used in remote controls. It has an efficient message queue where users can describe the waveform of a specific IR command in just a few bytes independently from the protocol.

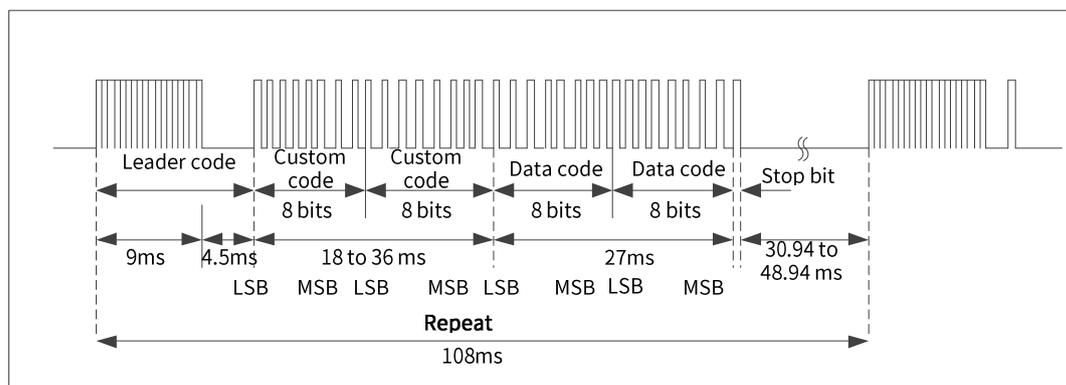
- Flexible carrier frequency and duty cycle.
- Flexible MARK and SPACE.
- Any IR remote control protocol.
- Supported 8 commands message queue in the FIFO.
- Interrupt report

Figure 19. Function block of IR Generator



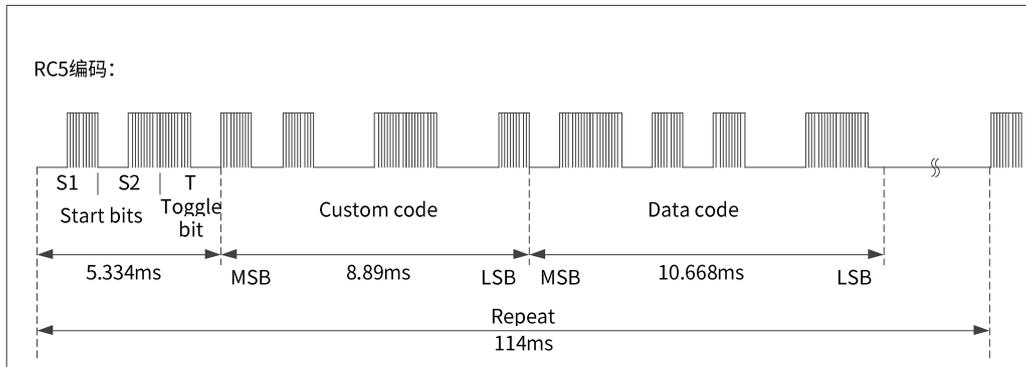
NEC code:

Figure 20. Waveform format of NEC code



RC5 code:

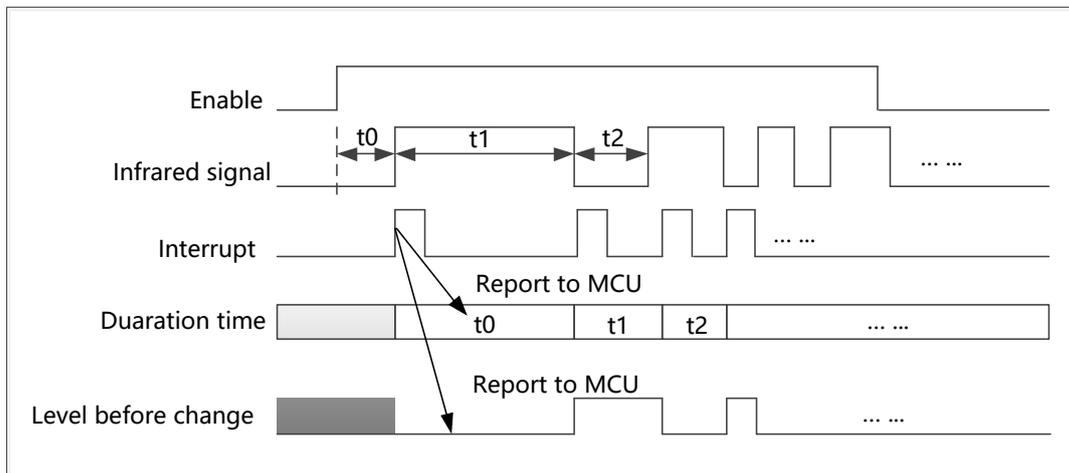
Figure 21. Waveform format of RC5 code



## IR Receiver

GW8811 series offer Infrared receiver can detect level change of infrared signal. When detect a level change, the receiver will trigger an interrupt to report MCU that the signal's level and duration time prior to the signal change for algorithm learning.

Figure 22. IR Receiver



### 3.13.7 Keyboard Scan

GW8811 series provides an 8x20 keyscan decoder for maximum 8 rows and 20 columns. The row and column could be assigned in specified IO for flexible configuration and layout.

When key is pressed, the keyscan circuit would auto scan the defined matrix and report to firmware in FIFOs.

### 3.13.8 Quadrature Decoder

GW8811 series provides a quadrature decoder for HID application. It could detect quadrature encoder signals and report to firmware in FIFOs. The decoder support sleep wakeup function.

### 3.13.9 PWM

GW8811KEU6 integrates 4 channels low speed PWM (32.768KHz) and 6 channels high speed PWM (the highest 32 MHz).

GW8811CEU6 integrates 3 channels low speed PWM (32.768KHz) and 3 channels high speed PWM (the highest 32 MHz).

#### High speed PWM

GW8811KEU6 integrates 6 channels high speed PWM with max. 32MHz clock, GW8811CEU6 integrates 3 channels high speed PWM with max. 32MHz clock. The characteristics are as following:

- The period can be configured (four channels are the same).
- Each channel can be configured its ratio and initial polarity independently.
- The period, duty cycle can be update dynamically (be in effect next period)
- The pulse could to be center-aligned or edge-aligned.

Figure 23. Center-aligned PWM

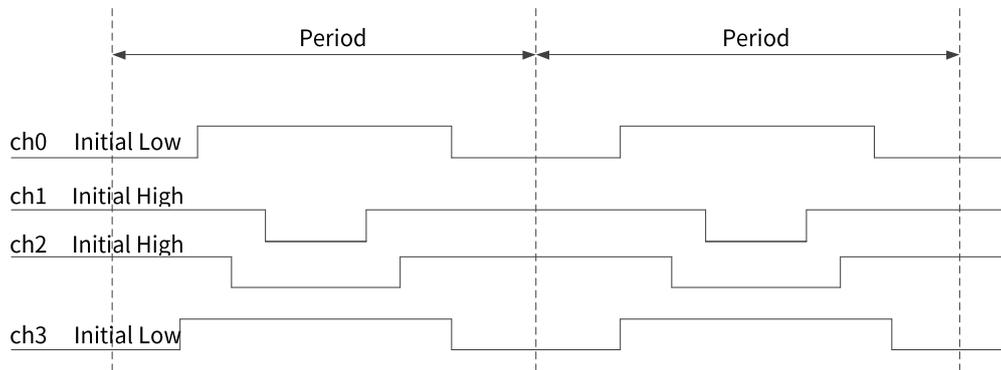
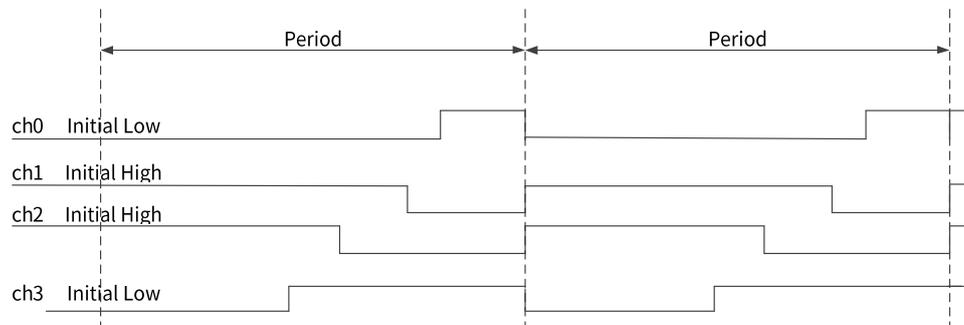


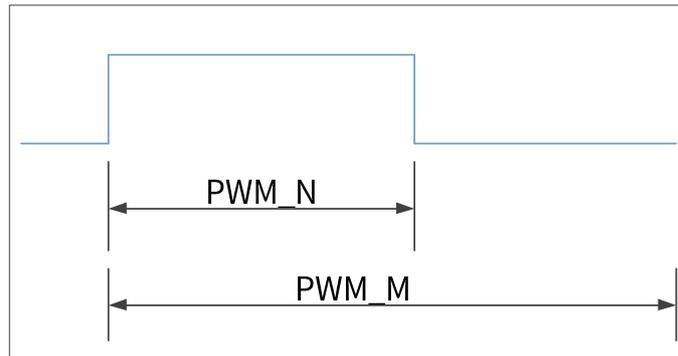
Figure 24. Edge-aligned PWM



### Low speed PWM (LED Controller)

GW8811KEU6 integrates 4 adjustable PWM generators while GW8811CEU6 integrates 3, and the both can be controlled by individual register and could be mux out at three different GPIOs. The minimum positive or negative width of PWM is 1/32ms and flexible setting ranges from 1 to 255 steps. Buzzer or LED dimming could be controlled by PWM signal with pre-defined PWM duty.

Figure 25. PWM Timing Setting Diagram



GW8811 series integrates LED controller which provide general On-OFF mode and Breathing light mode. The minimum LED on width is 1/32s with max 255 steps. LED ON-OFF repetition times could be configured as continuous or 1~127 times. Register table has setting description details. T1, T2, T3 are 8-bit width control register with minimum step 31.25ms.

For Breathing light mode, min, max, T4 are 8-bit width control register with minimum step 0.5ms. The sp is defined as breath mode speed with 4-bit width control register with minimum step, 31.25us.

Figure 26. LED ON-OFF Setting Diagram

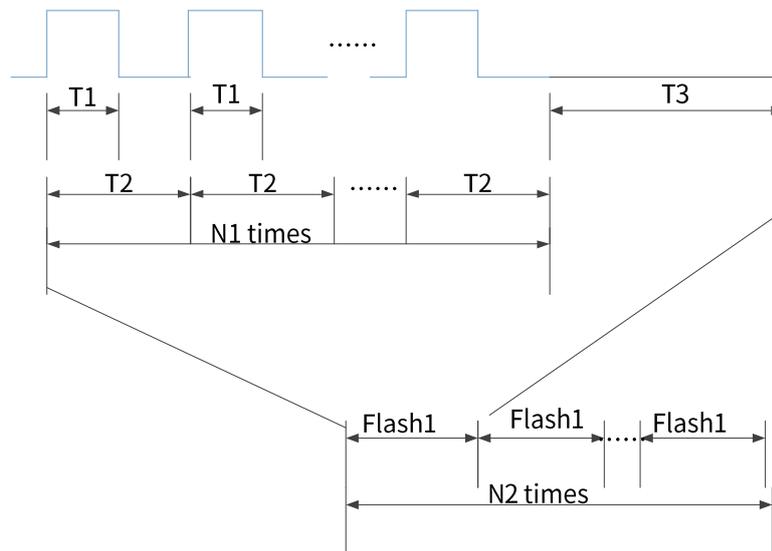
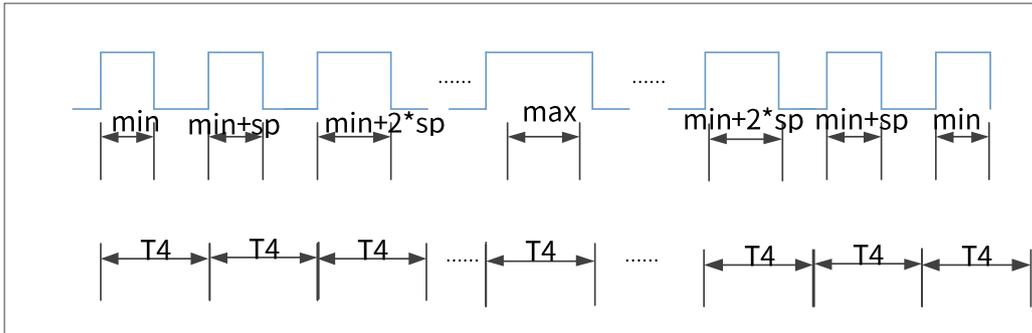


Figure 27. LED Breathing Light Setting Diagram



## 4 Pin characteristics

### 4.1 Pin Assignment and Signal Description

Figure 28. QFN32 pin assignments, top view (5mm\*5mm)

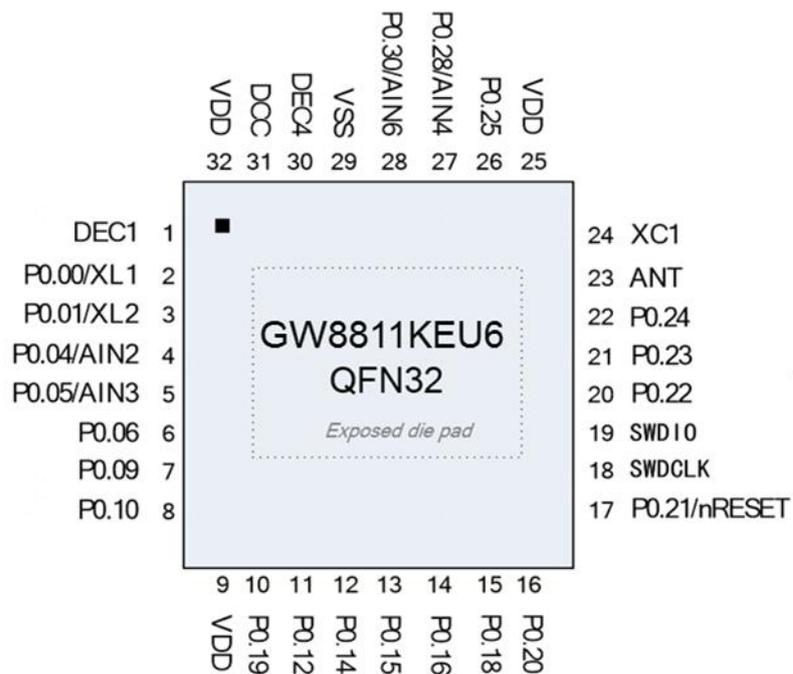


Table 5. QFN32 pin assignments

Pin	Name	Type	Description
<b>Left side of chip</b>			
1	1-Dec	Power	1.1 V regulator digital supply decoupling
2	P0.00	Digital I/O	General purpose I/O
	XL1	Analog input	Connection for 32.768 kHz crystal (LFXO)
3	P0.01	Digital I/O	General purpose I/O
	XL2	Analog input	Connection for 32.768 kHz crystal (LFXO)
4	P0.04	Digital I/O	General purpose I/O
	AIN2	Analog input	SAADC input
5	P0.05	Digital I/O	General purpose I/O
	AIN3	Analog input	SAADC input
6	P0.06	Digital I/O	General purpose I/O
			Capacitive touch
7	P0.09	Digital I/O	General purpose I/O
8	P0.10	Digital I/O	General purpose I/O
<b>Lower side of chip</b>			
9	VDD	Power	Power supply
10	P0.19	Digital I/O	General purpose I/O
11	P0.12	Digital I/O	General purpose I/O
12	P0.14	Digital I/O	General purpose I/O
13	P0.15	Digital I/O	General purpose I/O
14	P0.16	Digital I/O	General purpose I/O
15	P0.18	Digital I/O	General purpose I/O
16	P0.20	Digital I/O	General purpose I/O
<b>Right side of chip</b>			
17	P0.21	Digital I/O	General purpose I/O
	nRESET		Configurable as pin reset
18	SWDCLK	Digital input	Serial wire debug clock input for debug and programming
			Serial wire debug I/O for debug and programming
19	SWDIO	Digital I/O	Serial wire debug I/O for debug and programming
20	P0.22	Digital I/O	General purpose I/O
21	P0.23	Digital I/O	General purpose I/O
22	P0.24	Digital I/O	General purpose I/O
23	ANT	RF	Single-ended radio antenna connection
24	XC1	Analog input	Connection for 32 MHz crystal

Pin	Name	Type	Description
<b>Upper side of chip</b>			
25	VDD	Power	Power supply 1.8~3.6V
26	P0.25	Digital I/O	General purpose I/O
27	P0.28	Digital I/O	General purpose I/O
	AIN4	Analog input	Capacitive touch
			SAADC input
28	P0.30	Digital I/O	General purpose I/O
	AIN6	Analog input	Capacitive touch
			SAADC input
29	VSS	Power	Ground
30	4-Dec	Power	1.25 V power supply, output with 10uF or 4.7uf capacitance
31	DCC	Power	DCDC switch node, connect to DCDC inductance, high current path, keep PCB as wide and short as possible
32	VDD	Power	Power supply 1.8~3.6V
<b>Bottom of chip</b>			
Die pad	V <sub>SS</sub>	Power Ground pad	Exposed die pad must be connected
			to ground (V <sub>SS</sub> ), 9 or more via holes are recommended

## 4.2 QFN48 Pin Assignment and Signal Description

Figure 29. QFN48 pin assignments, top view (6mm\*6mm)

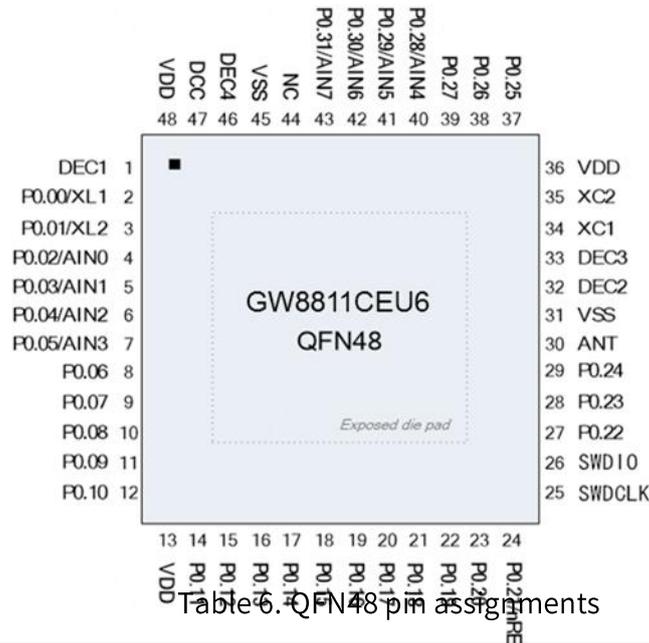


Table 6. QFN48 pin assignments

Pin	Name	Type	Description
<b>Left side of chip</b>			
1	1-Dec	Power	1.1 V regulator digital supply decoupling
2	P0.00	Digital I/O	General purpose I/O
	XL1	Analog input	Connection for 32.768 kHz crystal (LFXO)
3	P0.01	Digital I/O	General purpose I/O
	XL2	Analog input	Connection for 32.768 kHz crystal (LFXO)
4	P0.02	Digital I/O	General purpose I/O
	AIN0	Analog input	SAADC input
5	P0.03	Digital I/O	General purpose I/O
	AIN1	Analog input	SAADC input
6	P0.04	Digital I/O	General purpose I/O
	AIN2	Analog input	SAADC input
7	P0.05	Digital I/O	General purpose I/O
	AIN3	Analog input	SAADC input
8	P0.06	Digital I/O	General purpose I/O
			Capacitive touch
9	P0.07	Digital I/O	General purpose I/O
			Capacitive touch
10	P0.08	Digital I/O	General purpose I/O
			Capacitive touch

Pin	Name	Type	Description
11	P0.09	Digital I/O	General purpose I/O
12	P0.10	Digital I/O	General purpose I/O
<b>Lower side of chip</b>			
13	V <sub>DD</sub>	Power	Power supply 1.8~3.6V
14	P0.11	Digital I/O	General purpose I/O
15	P0.12	Digital I/O	General purpose I/O
16	P0.13	Digital I/O	General purpose I/O
17	P0.14	Digital I/O	General purpose I/O
18	P0.15	Digital I/O	General purpose I/O
19	P0.16	Digital I/O	General purpose I/O
20	P0.17	Digital I/O	General purpose I/O
21	P0.18	Digital I/O	General purpose I/O
22	P0.19	Digital I/O	General purpose I/O
23	P0.20	Digital I/O	General purpose I/O
24	P0.21	Digital I/O	General purpose I/O
	nRESET		Configurable as pin reset
<b>Right side of chip</b>			
25	SWDCLK	Digital input	Serial wire debug clock input for debug and programming
			Serial wire debug I/O for debug and programming
26	SWDIO	Digital I/O	Serial wire debug I/O for debug and programming
			Serial wire debug I/O for debug and programming
27	P0.22	Digital I/O	General purpose I/O
28	P0.23	Digital I/O	General purpose I/O
29	P0.24	Digital I/O	General purpose I/O
30	ANT	RF	Single-ended radio antenna connection
31	VSS	Power	Ground
32	2-Dec	Power	1.1 V RF supply with 0.1uf decoupling
33	3-Dec	Power	1.1V simulation supply with 0.1uf decoupling
34	XC1	Analog input	32 MHz crystal oscillator port 1(HFXO)
35	XC2	Analog input	32 MHz crystal oscillator port 2(HFXO)
36	VDD	Power	Power supply 1.8~3.6V
<b>Upper side of chip</b>			
37	P0.25	Digital I/O	General purpose I/O
38	P0.26	Digital I/O	General purpose I/O
39	P0.27	Digital I/O	General purpose I/O
40	P0.28	Digital I/O	General purpose I/O
	AIN4	Analog input	SAADC input

Pin	Name	Type	Description
41	P0.29	Digital I/O	General purpose I/O
	AIN5	Analog input	SAADC input
42	P0.30	Digital I/O	General purpose I/O
	AIN6	Analog input	SAADC input
43	P0.31	Digital I/O	General purpose I/O
	AIN7	Analog input	SAADC input
44	NC		Float
45	V <sub>SS</sub>	Power	Ground
46	4-Dec	Power	1.25 V power supply, output with 10uF or 4.7uf capacitance
47	DCC	Power	DCDC switch node, connect to DCDC inductance, high current path, keep PCB as wide and short as possible
48	V <sub>DD</sub>	Power	Power supply, 1.8~3.6V
<b>Bottom of chip</b>			
Die pad	V <sub>SS</sub>	Power Ground pad	Exposed die pad must be connected
			to ground (V <sub>SS</sub> ), 9 or more via holes are recommended

## 5 Electrical characteristics

### 5.1 Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Parameters	Symbol	Min	Max.	Unit	Notes
V <sub>DD</sub> Voltage	V <sub>DD</sub>	-0.4	V <sub>DD</sub> +0.3	V	
I/O Voltage	V <sub>DDIO</sub>	-0.4	V <sub>DDIO</sub> +0.3	V	
Relative Humidity	RH	0	50	%	Non-condensing, Non-biased
ESD	ESD <sub>HBM</sub>		2	kV	JESD22-A114E Standrad

**Notes:**

1. At room temperature.
2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability.
4. Functional operation under absolute maximum-rated conditions is not implied and should be restricted to the Recommended Operating Conditions.

## 5.2 Recommended Operating Conditions

Table 8. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature	T <sub>A</sub>	-40	25	85	°C	
Operating Junction Temperature	T <sub>J</sub>	-40	-	85	°C	
Power Supply Voltage	V <sub>VDD</sub>	1.8	3.3	3.6	V	Buck DCDC Power input supply. Includes overshoot
I/O Supply Voltage	V <sub>DD</sub>	1.8	3.3	3.6	V	Includes ripples
Regulator Output Voltage	V <sub>DEC1</sub>	0.9	1.1	1.2	V	Power for internal digital circuit
Serial Clock Frequency	SPI_CLK	-	-	32	MHz	
	I <sup>2</sup> C_SCL	-	4001	10002	KHz	

**Note:** GW8811KET6 does not guarantee the performance if the operating temperature is beyond the specified limit.

## 5.3 Temperature Range

Table 9. Temperature index

Parameters	Symbol	Min	Typ	Max.	Unit	Notes
Storage Temperature	T <sub>S</sub>	-40	-	85	°C	
Lead-free Solder Temperature	T <sub>P</sub>	-	-	245	°C	Refer to Package Handling Information document

## 5.4 DC Characteristics

Table 10. DC Electrical Specifications

Parameters	Symbol	Min	Typ.	Max	Unit	Conditions
DCDC Converter Input Voltage	$V_{VDD}$	1.8	3.3	3.6	V	
DCDC Converter Output Voltage	$V_{Buck\_OUT}$	1.1	1.25	-	V	
DCDC Converter Output Current	$I_{Buck\_Out}$	-	-	40	mA	Maximum output current under constant output voltage
DCDC Converter Output Ripple	$R_{Buck}$	-	30	-	mV	Peak to peak
<b>Power Consumption<sup>2</sup></b>						
TX RF Current @Pout = 0dBm			4.8		mA	@ $V_{VDD}$ = 3V with DCDC enable
RX RF Current @Sensitivity level			2.8		mA	@ $V_{VDD}$ = 3V with DCDC enable
Supply Current @ Sleep	$I_{SLEEP}$	-	2.7	-	$\mu$ A	@ $V_{VDD}$ = 3V with DCDC enable
Supply Current @ Deep sleep	$I_{PD}$	-	1	-	$\mu$ A	@ $V_{VDD}$ = 3V with DCDC enable

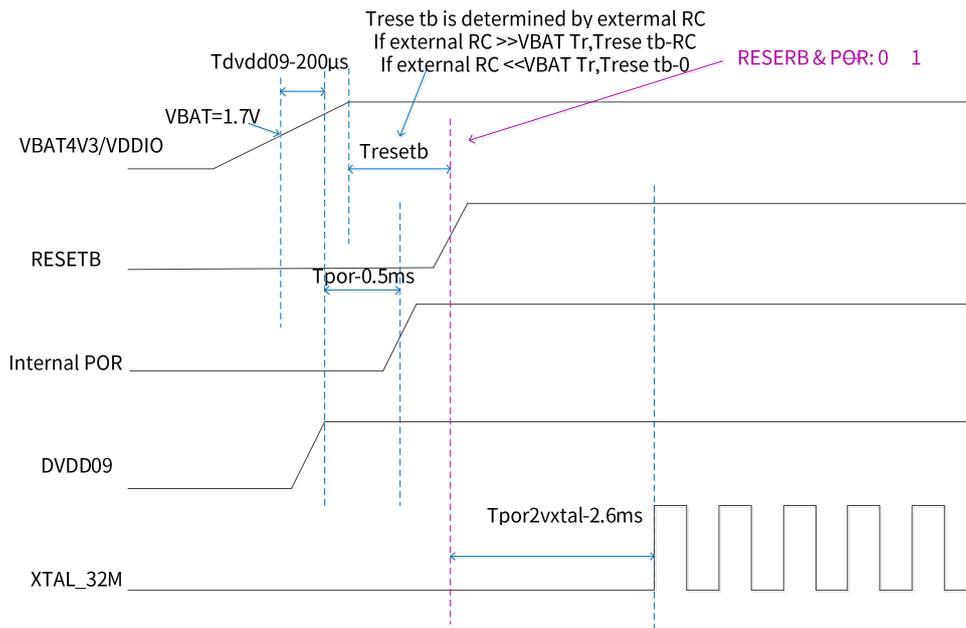
**Notes:**

1. Electrical Characteristics are defined under recommended operating conditions.
2. All the parameters are tested under operating conditions:  $V_{VDD}$  = 3.0V, DCDC Buck enable mode at  $T_A$  = 25°C.

## 5.5 AC and Timing Characteristics

### 5.5.1 Power-On Sequence

Figure 30. Power-On Sequence



### 5.5.2 32MHz Crystal Oscillator

The 32MHz Pierce crystal oscillator is designed for ultra-low power consumption and high stability. The 32MHz oscillator can be trimmed without external capacitors. Two digital controlled trimming loading capacitors are integrated and optimally designed for 10pF XTAL. Digital controlled capacitors could ease and speed up tuning procedure of XTAL frequency accuracy. The simplified schematic of the 32MHz crystal is shown in 0.

Figure 31. 32MHz Crystal Oscillator Circuit

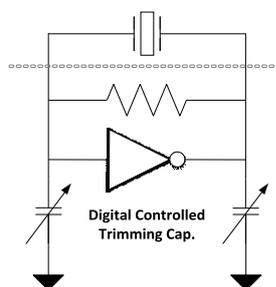


Table 11. 32MHz Crystal Oscillator Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
------------	--------	------	------	------	------	------------

Crystal Oscillator Frequency	$F_{X32M}$	-	32		MHz	
Crystal Oscillator Frequency tolerance	$F_{X32M\_TOL}$	-	<u>10</u>	<u>20</u>	ppm	Frequency tolerance depends on XTAL Spec.
Equivalent series Resistor	$ESR_{X32M}$		30	100	W	
Loading Capacitor	$C_{L\_X32M}$		9		pF	Built in digital controlled trimming loading cap, no external cap needed.
XTAL Drive Power	$P_{DRIVE\_X32M}$			100	uW	
XTAL OSC Start Up Time	$T_{START\_X32M}$		1.5	2.5	ms	

**Notes:** Electrical Characteristics are defined under recommended operating conditions

### 5.5.3 32.768kHz Crystal Oscillator

The 32.768 kHz oscillator is designed optimally for XTAL with C-Load =12.5pF , and no internal trimming capabilities and 32.768kHz clock is used as the clock source in the Sleep or Power Down modes.

Figure 32. 32.768kHz Crystal Oscillator Circuit

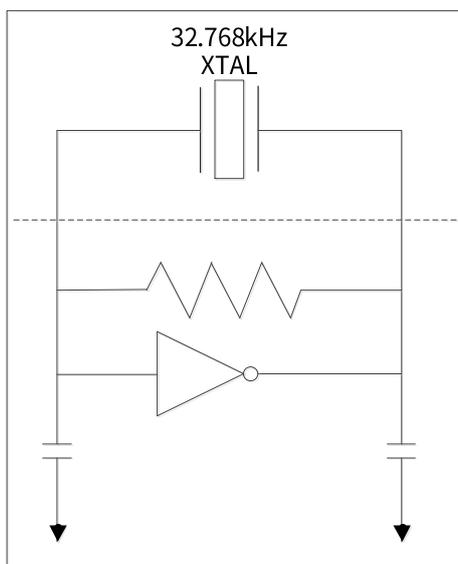


Table 12. 32.768kHz Crystal Oscillator Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Crystal Oscillator Frequency	$F_{X32k}$		32.768		kHz	
Crystal Oscillator Frequency tolerance	$F_{X32k\_TOL}$		<u>20</u>		ppm	
Equivalent series Resistor	$ESR_{X32k}$		50	80	k $\Omega$	
Load Capacitor	$C_{L\_X32k}$		12.5		pF	Built internal fixed load cap for 12.5pF XTAL
XTAL Drive Power	$P_{DRIVE\_X32k}$			1	$\mu$ W	
XTAL Start Up Time	$T_{START\_X32k}$		0.3	1	s	

#### 5.5.4 64MHz RC Oscillator

The 64MHz RC oscillator is designed for high speed wake up and high computing power application. Due to characteristic of RC oscillator, calibration is needed before switching to 64MHz RC oscillator mode. The 64MHz RC oscillator starts much faster than the 32MHz crystal oscillator.

Table 13. 64MHz RC Oscillator Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
RC Oscillator Frequency	$F_{RC64M}$		32		MHz	
RC Oscillator Frequency tolerance	$F_{RC64M\_TOL}$		<u>1</u>	<u>5</u>	%	
Oscillator Start Up Time	$T_{ST\_RC64M}$		2.5		us	

**Notes:** Electrical Characteristics are defined under recommended operating conditions

### 5.5.5 32.768kHz RC Oscillator

The 32.768kHz RC oscillator is designed for low cost applications without additional 32.768kHz XTAL. Due to characteristic of RC oscillator, calibration is needed before switching to 32.768kHz RC oscillator mode.

Table 14. 32.768kHz RC Oscillator Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
RC Oscillator Frequency	$F_{RC32k}$		32.768		kHz	
RC Oscillator Frequency tolerance	$F_{RC32k\_TOL}$		<u>2</u>		%	
RC Oscillator Frequency tolerance, Calibrated	$F_{RC32k\_TOL}$		<u>250</u>	<u>500</u>	ppm	Calibration needed before switching to RC oscillator mode
Start Up Time	$T_{START\_X32K}$		100		us	

**Notes:** Electrical Characteristics are defined under recommended operating conditions

## 5.6 RF Specifications

### 5.6.1 Transmitter RF Specification

Table 15. Transmitter Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency Range	FR <sub>TX</sub>	2402	-	2480	MHz	
Max. Output Power	P <sub>O,MAX</sub>	-		4	dBm	
Default Output Power	P <sub>O,DEF</sub>		0		dBm	
Output Power Adjust Range	P <sub>O,ADJ</sub>	-30		4	dBm	2dBm/step
Output Power Variation	P <sub>O,VAR</sub>		2		dBm	n
TX 20dB Bandwidth	BW <sub>20dB</sub>			1150	kHz	
1 <sup>st</sup> Adjacent Channel Power	P <sub>AJC1</sub>			-20	dBc	
2 <sup>nd</sup> Adjacent Channel Power	P <sub>AJC2</sub>			-40	dBc	
Delta F1 Frequency Deviation	Δf <sub>1AVG</sub>	225		275	kHz	
Delta F2 Frequency Deviation	Δf <sub>2AVG</sub>	185			kHz	
AVG Delta F2/ Delta F1	Δf <sub>AVG</sub>	0.8				Δf <sub>2AVG</sub> /Δf <sub>1AVG</sub>
Frequency Offset	F <sub>OFFSET</sub>	-150		150	kHz	
Carrier Frequency Drift	CF <sub>DRIFT</sub>			50	kHz	
Carrier Frequency Drift rate	CF <sub>DRIFT_Rate</sub>			20	kHz/50μs	
2 <sup>nd</sup> Harmonics Power Level	Har <sub>2nd</sub>			-40	dBm	@Pout = 0dBm
3 <sup>rd</sup> Harmonics Power Level	Har <sub>3rd</sub>			-45	dBm	@Pout = 0dBm

Notes: Electrical Characteristics are measured under BLE specification and

recommended operating conditions

## 5.6.2 Receiver RF Specification

Table 16. Receiver Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency Range	FR <sub>RX</sub>	2402		2480	MHz	
Maximum Input Power	RX <sub>MAX</sub>		0		dBm	With PER <30.8%
Ideal Signal Sensitivity	SEN <sub>IDEAL</sub>		-94		dBm	
Dirty Signal Sensitivity	SEN <sub>DIRTY</sub>		-92		dBm	
<b>C/I and Selectivity</b>						
C/I Co-Channel	C/I <sub>CO</sub>		9		dB	
C/I Adjacent +1MHz	C/I <sub>1M</sub>		-1		dB	
C/I Adjacent +2MHz	C/I <sub>2M</sub>		-38		dB	
C/I Adjacent ≥ +3MHz	C/I <sub>3M</sub>		-48		dB	
C/I Image Channel	C/I <sub>IMG</sub>		-25		dB	
C/I Image+1M Channel	C/I <sub>IMG+1M</sub>		-35		dB	
<b>Inter-Modulation Performance</b>						
IMD performance	IMD		-24		dBm	3rd, 4th and 5th offset channel
<b>Blocking Performance</b>						
Blocking 30~2000MHz	P <sub>BLK_30~2000MHz</sub>	-10			dBm	
Blocking 2003~2399MHz	P <sub>BLK_2003~2399MHz</sub>	-30			dBm	
Blocking 2484~2997MHz	P <sub>BLK_2484~2997MHz</sub>	-30			dBm	
Blocking 3000MHz~12.75GHz	P <sub>BLK_3~12.75GHz</sub>	-10			dBm	

**Notes:** Electrical Characteristics are measured under BLE specification and recommended operating conditions

## 6 Design References

### 6.1 Application Schematics

#### 6.1.1 GW8811KEU6 Reference Application Circuit

Figure 33. GW8811KEU6 Reference Application Circuit (32.768k xtal is optional)

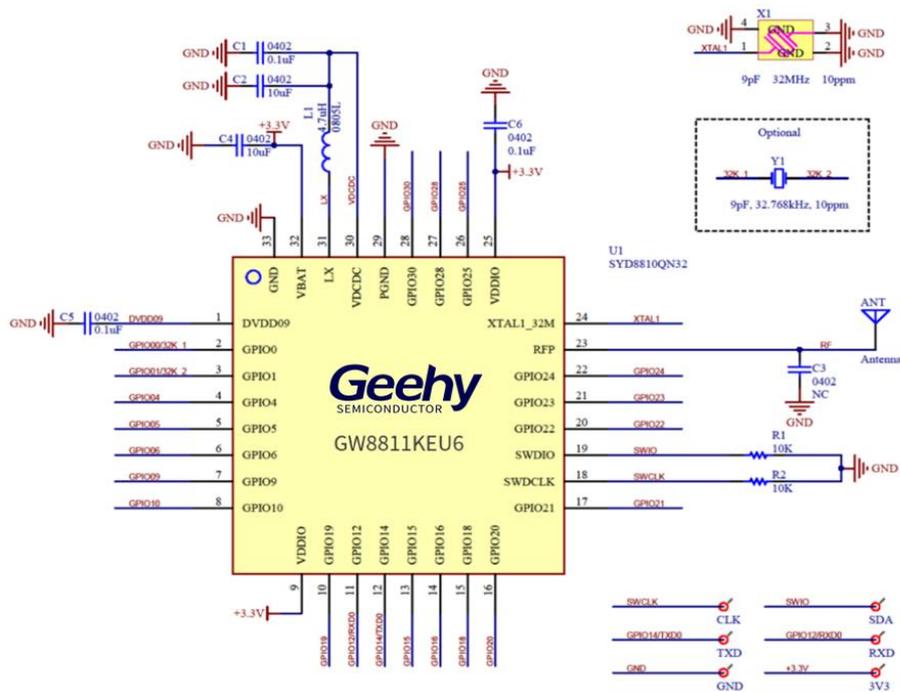


Table 17. BOM of GW8811KEU6

Designator	Value	Description	Footprint
C4, C5	100 nF	Capacitor, X5R, $\pm 20\%$	402
C9	4.7 $\mu$ F	Capacitor, X5R, $\pm 20\%$	0603 or 0402
C10	10 $\mu$ F recommended	Capacitor, X5R, $\pm 20\%$	603
L2	4.7 $\mu$ H	Inductor, IDC, min = 30 mA, $\pm 20\%$	603
U1	GW8811KEU6	ULP Bluetooth low energy SoC	QFN48
X1	32 MHz	32 MHz, CL = 10 pF, Tol: $\pm 10$ ppm	3225
X2 (optional)	32.768 kHz	32.768 kHz, CL = 12.5 pF, Tol: $\pm 20$ ppm	3215

### 6.1.2 GW8811CEU6 Reference Application Circuit

Figure 34. GW8811CEU6 Reference Application Circuit

(32.768k xtal is optional)

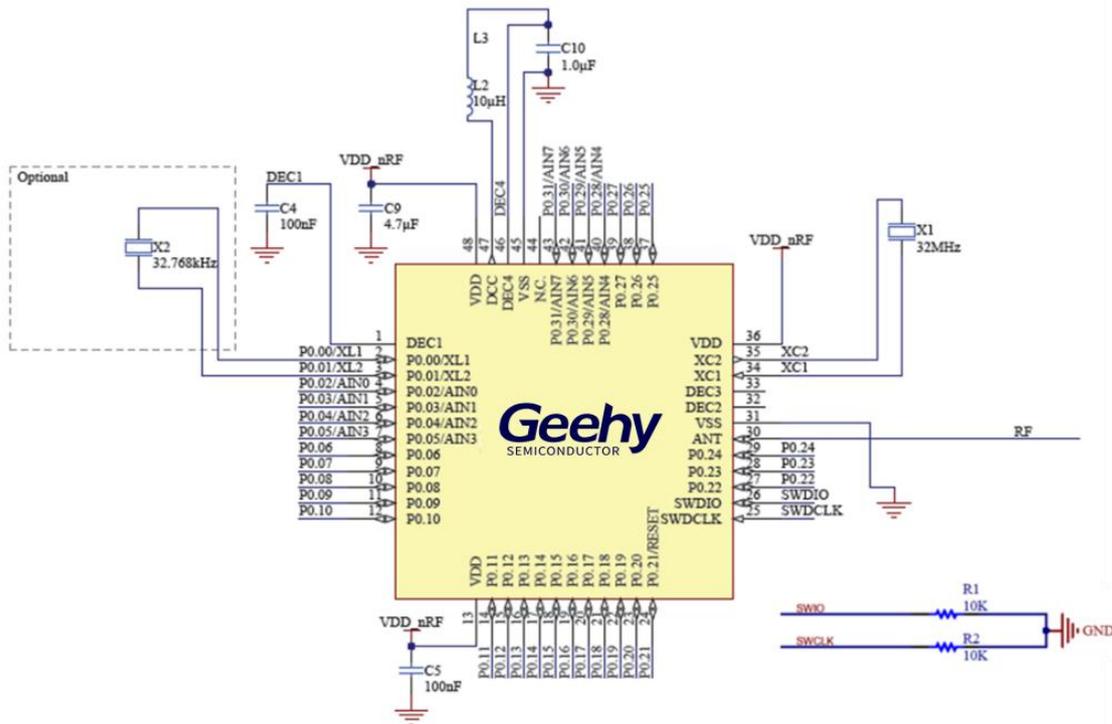


Table 18. BOM of GW8811CEU6

Designator	Value	Description	Footprint
C4, C5	100 nF	Capacitor, X5R, ±20%	402
C9	4.7 µF	Capacitor, X5R, ±20%	0603 or 0402
C10	10 µF recommended	Capacitor, X5R, ±20%	603
L2	4.7 µH	Inductor, IDC,min = 30 mA, ±20%	603
U1	GW8811CEU6	ULP Bluetooth low energy SoC	QFN48
X1	32 MHz	32 MHz, CL = 10 pF, Tol:±10ppm	3225
X2 (optional)	32.768 kHz	32.768 kHz, CL = 12.5 pF, Tol: ±20 ppm	3215

## 6.2 Layout Design Guidelines

**Precaution:** PCB layout is extremely important to minimize parasitical capacitance and improve RF performance.

The following layout guidelines are recommended to achieve optimum performance.

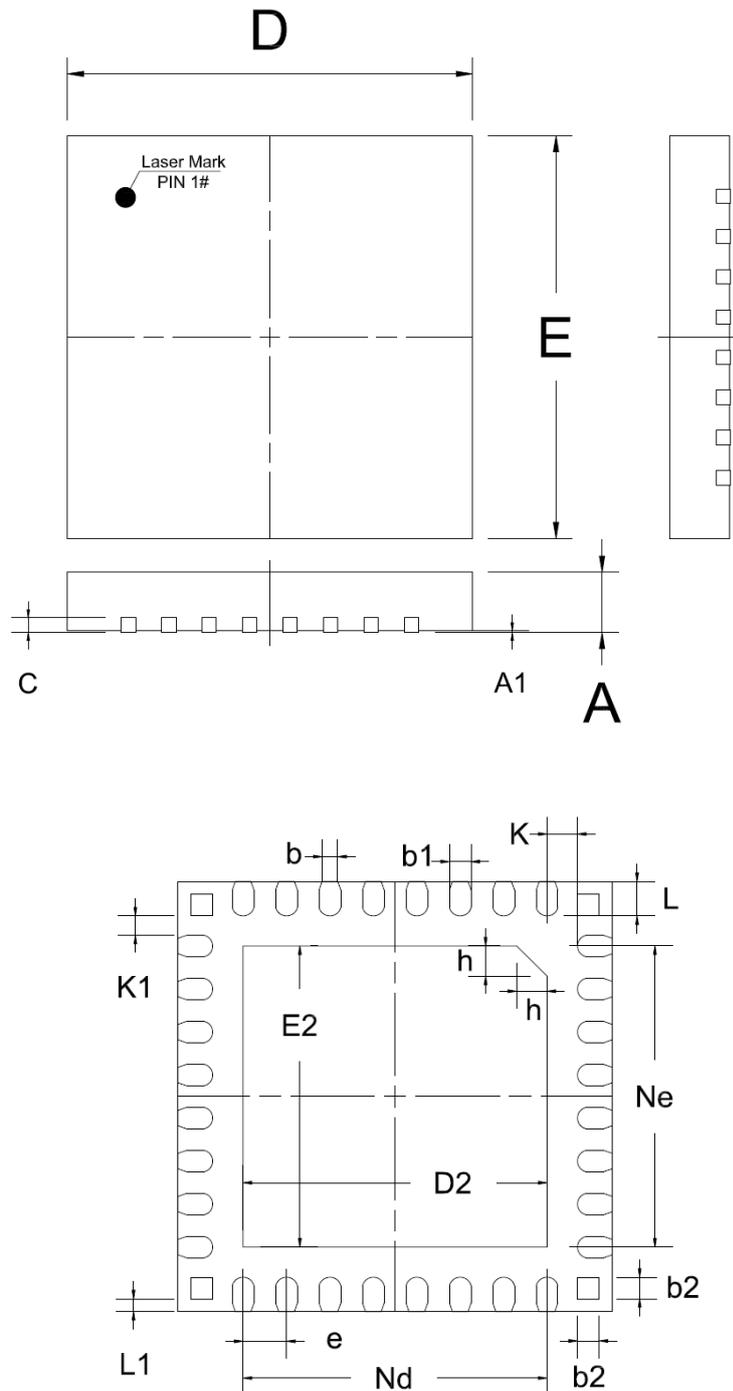
1. Make sure RF 50-ohm trace is with GND continuation.
2. Place the DCDC inductor close to the DCC pin. Keep the traces short and wide enough.
3. Place the decoupling capacitor C10 close to the DEC4 PIN.
4. Route PIN45 VSS to gnd plane by VIA (4layer PCB) , or route PIN45 VSS to bottom layer by VIA (2layer PCB), DO NOT connect PIN45 VSS to top layer gnd; \*\* PIN45 VSS is dirty DCDC gnd.
5. Place passive crystal oscillator as close as possible to the oscillator pins to reduce the parasitic capacitance and the interference to other circuits.
6. Ensure that the ground plane under the oscillator and its components are in good quality.
7. Avoid long connections to the passive crystal and also to the load capacitor which may create a large loop on the PCB.
8. Do not route any digital-signal lines on the opposite side of the PCB under the RF trace and crystal area.
9. Keep other digital signal lines, especially clock lines and frequently switching signal lines, as far away from crystal/analog/RF connections as possible.
10. Place at least 9 ground VIAs directly under QFN thermal PAD for good grounding and thermal dissipation.

## 7 Package information

### 7.1 GW8811KEU6 Package

#### 7.1.1 Package Size

Figure 35. Outline and dimensions of gw8811keu6 package



Apexmic	MILLMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
b	0.2	0.25	0.3
b1	0.18REF		
b2	0.2	0.25	0.3
c	0.203REF		
D	4.9	5	5.1
D2	3.4	3.5	3.6
e	0.50BSC		
Nd	3.50BSC		
Ne	3.50BSC		
E	4.9	5	5.1
E2	3.4	3.5	3.6
L	0.35	0.4	0.45
L1	0.15REF		
h	0.3	0.35	0.4
K	0.35REF		
K1	0.225REF		

### 7.1.2 Package Marking

Refer to for the code marking location on the device package.

Figure 36. Package Marking



Table 19. Code Identification

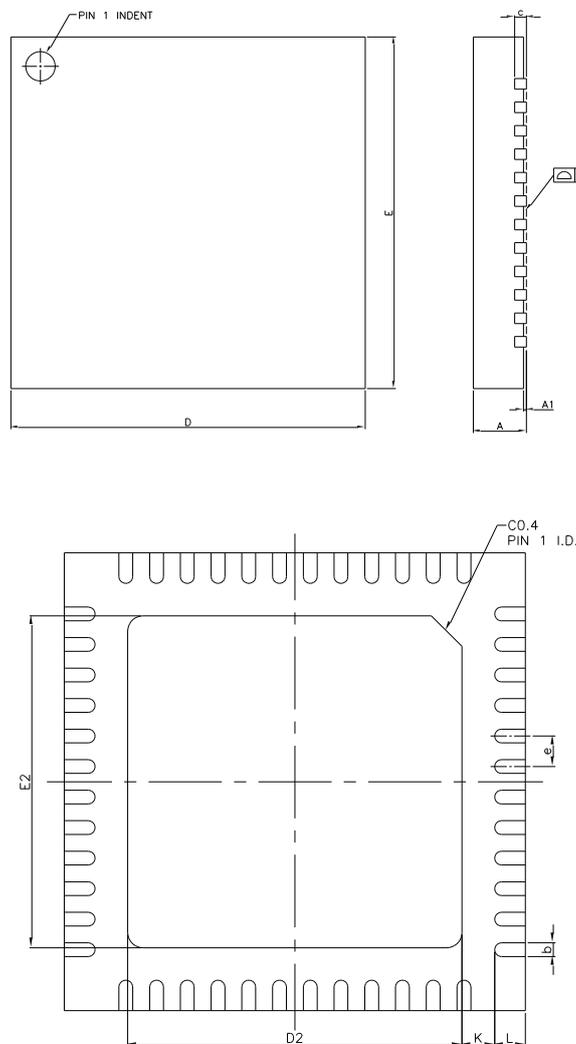
Marking	Description
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LYWWXXXXXXXX	GW8810KEU6 Date Code
	Y: Assembly year
	e.g. (Yearly 2018) -> 8
	WW: Assembly week
	e.g. (Weekly 16) -> 16
	XXXXX: NO.
	e.g. 433CE12

## 7.2 GW8811CEU6 Packaging

### 7.2.1 Mechanical Dimension

Figure 37. GW8811CEU6 Package Outline Diagram and Dimension



SYMBOLS	DIMENSIONS IN MILLIMETERS
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	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	- - -	0.20REF	- - -
D	5.90	6.00	6.10
D2	4.30	4.35	4.40
E	5.90	6.00	6.10
E2	4.30	4.35	4.40
e	- - -	0.40	- - -
K	- - -	0.425REF	- - -
L	0.350	0.400	0.450
y	0.00	- - -	0.075

### 5.2.2 Package Marking

Refer to Figure 38 for the code marking location on the device package.

Figure 38. Package Marking



Table 20. Code Identification

Marking	Description
LYWWXXXXXXXX	GW8810CEU6 Date Code
	Y: Assembly year
	e.g. (Yearly 2018) -> 8
	WW: Assembly week
	e.g. (Weekly 16) -> 16
	XXXXX: NO.
	e.g. 433CE12

## 8 Ordering information

Part number	Package	Packing	Minimum Order Quantity
GW8811KEU6	QFN 5mmx5mm 32-Pin	Tape Reel	3K
GW8811CEU6	QFN 6mmx6mm 48-Pin	Tape Reel	3K

## 9 Document Revision History

Revision Number	Date	Description
1.0.1	4.23.2020	NEW